IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Timothy A. Rost	Docket No.:	TI-36595
Serial No.:	10/785,648	Art Unit:	2814
Filing Date:	February 24, 2004	Examiner:	Pham, Long
Customer No.:	23494	Conf. No.:	3709

Title: Transistor Design and Layout for Performance Improvement with Strain

RESPONSE UNDER 37 CFR 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following remarks are offered in response to the Examiner's Office Action dated March 14, 2007. They are respectfully submitted as a full and complete response to that Action.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 9-18 are pending in this case.

The Examiner rejected claims 9-18 under 35 U.S.C.§ 103(a) as being unpatentable over Ouyang et al. (U.S. Pub. 2004/0256639) in combination with Lin et al. (U.S. Pub. 2005/0035369), Yeo et al. (U.S. Pub. 2005/0009263), Chidambarrao et al. (U.S. Pub. 2005/0164477), and Currie et al. (U.S. Pub. 2004/0173812).

Applicant respectfully submits that claim 9 is patentable over the references as there is no disclosure or suggestion in the references of forming PMOS devices with entire source to drain channel regions formed within the substrate along a first crystallographic orientation axis, forming NMOS devices with entire source to drain channel regions formed within the substrate along a second crystallographic orientation axis of the semiconductor substrate, applying a compressive strain longitudinally across the source to drain channel regions of the PMOS devices, and applying a tensile strain longitudinally across the source to drain channel regions of the NMOS devices. Ouyang teaches a vertical nMOSFET rotated from a vertical pMOSFET. While acknowledging planar transistors, Ouyang teaches against using planar transistors. The Examiner applies Lin to teach lateral PMOS and NMOS transistors and argues that it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Lin into the method of Ouyang to obtain the advantages of increased mobility (due to straining of the channel) and size reduction (due to formation of lateral PMOS and NMOS). However, one of the reasons taught by Ouyang against using planar transistors is that the channel length is limited by lithography (paragraph [0007]). Ouyang further teaches that the limitation of channel length reduction can be solved if vertical transistors are used instead. Given this teaching, one of ordinary skill in the art would not be motivated to use lateral transistors of Lin for the purpose of size reduction as suggested by the Examiner. Since the teachings of the references taken as a whole do not suggest size reduction is obtained using lateral transistors, it would not have been obvious to one of ordinary skill in the art to incorporate the teachings of Lin et al into the method of Ouyang. Accordingly, Applicant respectfully submits that claim 9 and the claims dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 9-18. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

/Jacqueline J Garner/

Jacqueline J. Garner
Reg. No. 36,144

Texas Instruments Incorporated
P. O. Box 655474, M.S. 3999
Dallas, Texas 75265
Phone: (214) 532-9348
Fax: (972) 917-4418